To: Ms. ANNETTE M THOMPSON
Patent Examiner Art Unit : 2825
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Ms. Annette M. Thompson :

(Subject : This Patent Application is already prior art and has been in practice since 1990 and widely used in most universities around our blessed country and abroad and also commercially utilized as software program "misII" and "sis-1.2" originally written at University of California at Berkeley mainly by master's and doctoral students since 1990 of Professor Robert Brayton tel : (510) 643 9801 email: **brayton**@eecs.**berkeley**.edu and Professor Alberto Sangiovanni-Vincentelli email **alberto**@eecs.**berkeley**.edu tel: (510) 642-4882). These inventors are cunningly defrauding our country by trying to patent a software already in use as is - Please reject this application.

Application Publication Number : US **20020069396** A1
Entitled, "Method for automated design of integrated circuits with targeted quality objectives using dynamically generated building blocks"

Inventors: **Bhattacharya, Debashis**; *(Plano, TX)* ; **Boppana, Vamsi**; *(Santa Clara, CA)* ; **Roy, Rabindra K.**; *(Hillsboro, OR)* ; **Roy, Jayanta**; *(San Jose, CA)*
Patent Application # 09/896,059

---------- Follow-on to **Rejected** begin ----------
(As a follow up of ***rejected*** Application # 09/896,071;
Rejected publication # US 2002-0053063 A1 ;
Inventors of **Rejected** Application: **Bhattacharya, Debashis**; *(Plano, TX)* ; **Boppana, Vamsi**; *(Santa Clara, CA)* ; **Murgai, Rajeev**; *(Santa Clara, CA)* ; **Roy, Rabindra**; *(Hillsboro, OR)* ;
Rejected title : Process for automated generation of design-specific complex functional blocks to improve quality of synthesized digital integrated circuits in CMOS)
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Publications related to this publication number : US **20020069396** A1

* This publication is largely the basis of transistor level design where the rest of the design may be standard cells :
checked
Title **"Logic synthesis for large pass transistor circuits"** International Conference on Computer Aided Design, Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design, San Jose, California, United States Pages: 663 - 670 Year of Publication: 1997 ISBN:0-8186-8200-0 ; Authors Premal Buch ; Amit Narayan; A. Richard Newton; A. Sangiovanni-Vincentelli

** This publication includes partitioning software commands "xl_partition" and "xl_k_decomp" written by Mr. R. Murgai (an inventor to rejected publication US 2002-0053063 A1 & not included in Publication # US **20020069396** A1 as the core basis for this application :
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E. M. Sentovich, K. J. Singh, L. Lavagno, C. Moon, R. **Murgai**, A. Saldanha, H. Savoj, P. R. Stephan, R. K. Brayton, and A. Sangiovanni-Vincentelli, "SIS: A System for Sequential Circuit Synthesis," Memorandum UCB/ERL M92/41, Univ. of California, Berkeley, May 1992

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